A.3: New Trigger Generator Unit for Microtron Timing Controls

Trigger generator unit has been used for generating the Master trigger (MST) and other timing instants for the operation of Microtron and associated subsystems, in a sequential manner. The earlier trigger generator had undergone many modifications to meet different requirements that came up in course of time. Requirements of new triggering instants for RF modulator were also added. The module was redesigned in Accelerator Control Section (ACS) to take care of all the new demands along with the existing requirements.

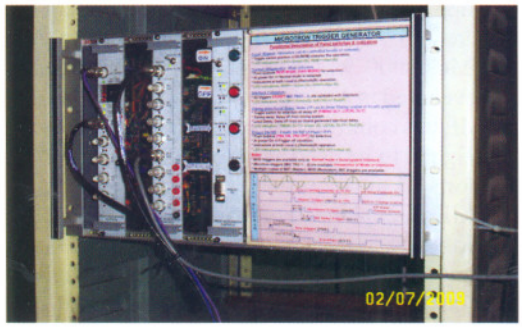

Fig. A.3.1: The Trigger Generator

The design supports generation of main accelerator trigger/Master trigger of programmable PRR (Pulse Repetition Rate). MST is derived from the 50 Hz pulse train at zero crossing instant of the cathode current. This 50 Hz signal is scaled down to 1 Hz in synchronism to zero crossing instant. MST is sent to Indus-1 timing control system, which in turn generates a delayed trigger for the beam injection and sends it back to trigger generator.

The delayed trigger is sent to RF modulator after isolation by trigger generator. Programmable pre trigger with respect to MST and delayed trigger with respect to modulator trigger are also generated. All the trigger outputs are of TTL level with 50 driving capacity. Galvanically isolated outputs are used to meet both channel-to-channel and input to output isolation. Multiple trigger outputs are generated for each trigger signal. Normal and diagnostics modes of operation, along with selectable trigger on/off facility have been provided. All the triggers are qualified with good system interlock conditions at normal mode. In diagnostics mode, only MST and delayed trigger are produced locally to perform any test but modulator trigger is not generated.

The developed trigger generator is modular in nature. Different boards have been designed for generating different timing instants. These boards are connected via a common back plane. All the trigger signals are made available at the backplane. With this, the system expandability becomes easier. I/O connectivity, test points, LED indications and control push buttons are provided on the front panel. The trigger generator has been deployed in Microtron Control System after a rigorous testing in lab and is working satisfactorily. Measured rise time of trigger outputs with 100 meter cable on 50 termination is ~ 40ns. Jitter and voltage droop are measured as less than 10 ns and 12% respectively.

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A.4: Development of Pulsed Kicker Magnets for Indus-2

Injection system of Indus-2 consists of Pulsed thin & thick septum magnets and four Kicker Magnets. Injection of 600 MeV electrons into the Storage ring in the horizontal plane is carried out by combination of these pulsed magnets. In this report, a brief overview of Pulsed Kicker magnet development for injection of 600 MeV electrons into Indus-2 ring is given.

Window type, electrically lumped kicker magnets are chosen on the basis of good field spatial homogeneity, low leakages, & pulser simplicity. Magnetic design simulation have been carried out using Flux2D & transient OPERA 3D. Main parameters of kicker magnets are shown in Table A.4.1.

Each magnet has been constructed in window frame, single turn coil with Ni-Zn-Co ferrites mounted around ceramic chamber Their assembly details are shown in Fig. A.4.1.

Table A.4.1: Main parameters of the kicker magnets

Injection Energy	700 MeV
Magnet deflection	25 mrad
Magnet aperture	130 mm H x 65 mm V
Magnet length	300 mm
Magnet field	0.22 T at @11 KA
Magnet pulse field shape	Half sine wave - 3 ms

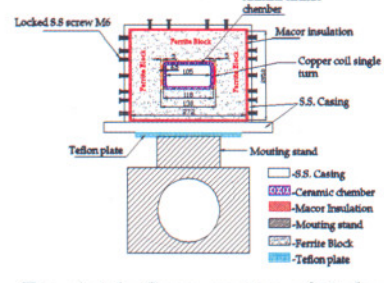

Fig. A.4.1: Cross section of Kicker magnet

A new resonance model of ferrite assembly for kicker magnet impedance has been developed. The model is cylindrically symmetric with ferrite surrounding the beam aperture. The longitudinal impedance of a kicker magnet with titanium coated ceramic chamber has been measured from 0.3 to 100 MHz using RF network analyzer. The real part of the impedance has a peak value of about 1Ω around 30 MHz, which decreases monotonously when the frequency increases. Measured longitudinal coupling impedance is in good agreement with resonance model. The inner surfaces of the ceramic chambers were coated with Titanium conducting layer to reduce beam coupling impedance and provides passage for beam image current. Titanium coating thickness has been measured by a concentric circular probe developed in our lab.

Magnetic attenuation and phase delay of kicker field pulse have been measured. It is observed that attenuation is ~ 1- 2 %, and phase delay is ~ 60 - 80 ns. Magnetic field in the mid-plane of a kicker magnet was measured with metallized ceramic chamber. Field homogeneity (ΔB/Bo) in the order of ~ 5 x 10^{-3} has been observed. Magnetic field distribution in kicker aperture along longitudinal axis (beam path) is shown in Fig. A.4.2.

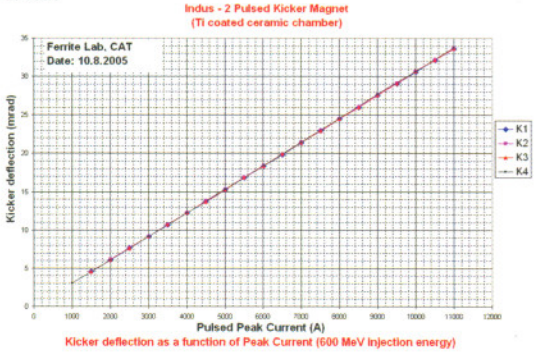

Fig. A.4.2: Magnetic field distribution in gap along magnet length

The linearity of kicker deflection versus the peak current is shown in Fig. A.4.3.

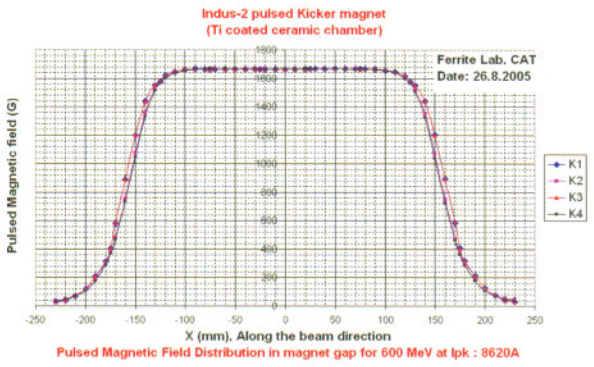

Fig. A.4.3: Linearity response of kicker magnets

Magnetic field stability of about 0.2 % with floated body at 30 KV/10 KA has been observed. Pulsed kicker magnets are working satisfactorily for the injection of 550-600 MeV electrons into 2.5 GeV Storage ring during Indus-2 operations.

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A.5: New VME bus based CPU card CPU68K-2PORT for Indus controls

The upgradation of Indus-1 Control system has been recently taken up. As a first step towards it, a new CPU board based on MC68000 which is a 16 bit microprocessor was recently developed in Accelerator Control Section (ACS). It is used as VME bus controller for control sub systems of Iundus-1. It is designed to be used as single master on the VME bus and supports 24 bit addressing, and uses only P1 connector for the VME backplane. For ease-of use, the CPU has a resident firmware package that provides a self-contained programming and operating environment. The operating environment provided by this firmware contains monitor/debugger, assembly/disassembly, program entry and I/O control functions.

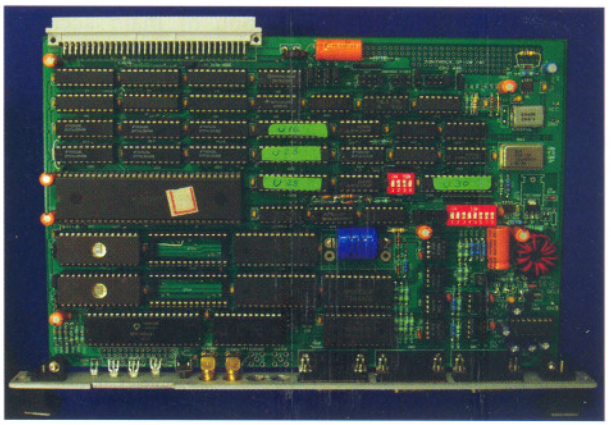

Fig. A.5.1: VME CPU card - CPU68K-2PORT

Features: It is a new upgraded version of the CPU−68K and supports the TUTOR 1.4 version of monitor. The address map of the various devices used on the board is in conformance with the addresses referred in the TUTOR monitor for the same functional devices.

On board memory : It has 32 KB [16 KB (Even) + 16KB (Odd)] EPROM which includes about 20 KB of TUTOR monitor and 16 KB [8 KB (Even) + 8 KB (Odd)] RAM, of which 4 KB is used by the monitor. It has optional memory