A new resonance model of ferrite assembly for kicker magnet impedance has been developed. The model is cylindrically symmetric with ferrite surrounding the beam aperture. The longitudinal impedance of a kicker magnet with titanium coated ceramic chamber has been measured from 0.3 to 100 MHz using RF network analyzer. The real part of the impedance has a peak value of about 1Ω around 30 MHz, which decreases monotonously when the frequency increases. Measured longitudinal coupling impedance is in good agreement with resonance model. The inner surfaces of the ceramic chambers were coated with Titanium conducting layer to reduce beam coupling impedance and provides passage for beam image current. Titanium coating thickness has been measured by a concentric circular probe developed in our lab.

Magnetic attenuation and phase delay of kicker field pulse have been measured. It is observed that attenuation is ~ 1- 2 %, and phase delay is ~ 60 - 80 ns. Magnetic field in the mid-plane of a kicker magnet was measured with metallized ceramic chamber. Field homogeneity (ΔB/Bo) in the order of ~ 5 x 10^{-3} has been observed. Magnetic field distribution in kicker aperture along longitudinal axis (beam path) is shown in Fig. A.4.2.

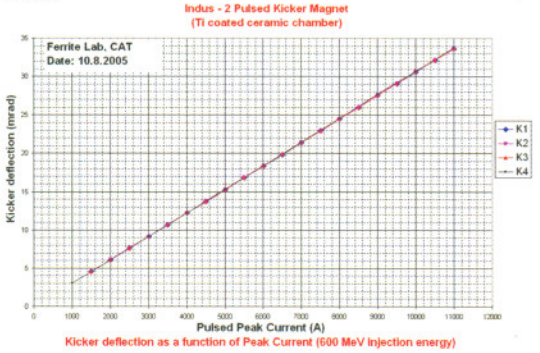

Fig. A.4.2: Magnetic field distribution in gap along magnet length

The linearity of kicker deflection versus the peak current is shown in Fig. A.4.3.

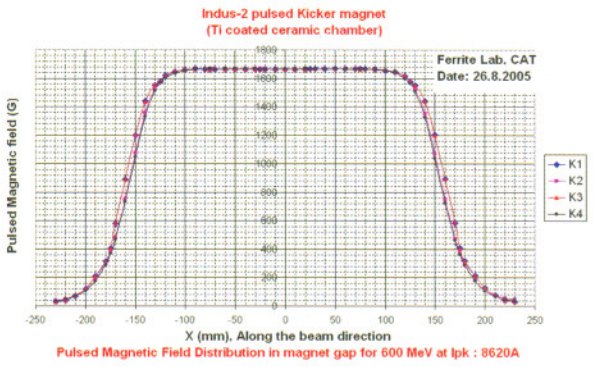

Fig. A.4.3: Linearity response of kicker magnets

Magnetic field stability of about 0.2 % with floated body at 30 KV/10 KA has been observed. Pulsed kicker magnets are working satisfactorily for the injection of 550-600 MeV electrons into 2.5 GeV Storage ring during Indus-2 operations.

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A.5: New VME bus based CPU card CPU68K-2PORT for Indus controls

The upgradation of Indus-1 Control system has been recently taken up. As a first step towards it, a new CPU board based on MC68000 which is a 16 bit microprocessor was recently developed in Accelerator Control Section (ACS). It is used as VME bus controller for control sub systems of Iundus-1. It is designed to be used as single master on the VME bus and supports 24 bit addressing, and uses only P1 connector for the VME backplane. For ease-of use, the CPU has a resident firmware package that provides a self-contained programming and operating environment. The operating environment provided by this firmware contains monitor/debugger, assembly/disassembly, program entry and I/O control functions.

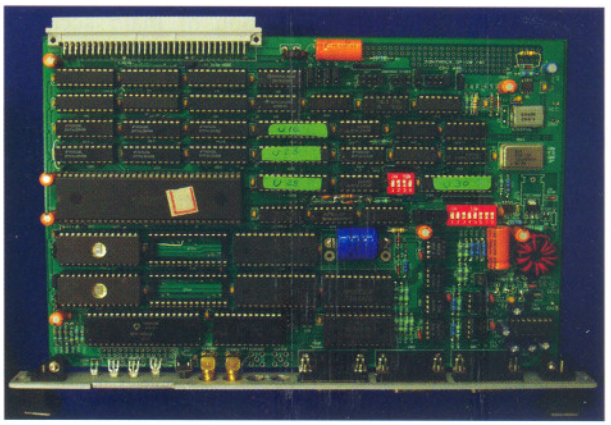

Fig. A.5.1: VME CPU card - CPU68K-2PORT

Features: It is a new upgraded version of the CPU−68K and supports the TUTOR 1.4 version of monitor. The address map of the various devices used on the board is in conformance with the addresses referred in the TUTOR monitor for the same functional devices.

On board memory : It has 32 KB [16 KB (Even) + 16KB (Odd)] EPROM which includes about 20 KB of TUTOR monitor and 16 KB [8 KB (Even) + 8 KB (Odd)] RAM, of which 4 KB is used by the monitor. It has optional memory

sockets to house 16 KB [8 KB (Even) + 8 KB (Odd)] of memory. Either 8 or 16 KB RAM or EPROM can be used as optional memory. Various optional memory usages are jumper configurable. 512 KB memory space is reserved for onboard memory and devices. Rest of the 16 MB is available for use on VME bus.

Serial Ports: The board is equipped with two serial ports. Both can have independent baud rates in binary starting from 1200 baud up to 76.3 Kb. Baud rates are set by DIP switch. The RS232 drivers for both the ports are powered from isolated power generated onboard. The ports can be configured as independent RS232 ports or any of the two ports can be used as RS485 port for 2-wire variant. DIP switches and some of the jumpers are configured for this option. RS485 port is also driven by isolated power. Both the ports can work in normal as well as in interrupt mode.

Timers: The board has three onboard timers. One of the timers is fed with 4.9152 MHz clock whereas other two are available as general purpose timers. They can be cascaded, used independently or can be used as dividers for generating other clocks. The clock out from these two timers is also available on facia. These can be programmed to divide the TTL square wave input from the facia connectors. Timer clock O/P can be used to generate events for triggering any I/O boards for synchronized reading. The timers can be used to interrupt the CPU like timer tick, or on multiples of external events. The timer operation can be enabled or disabled. All the options are jumper selectable.

Parallel Ports: Two parallel ports and some bit programmable (generally used as hand shake) signals are provided.

Interrupts: Normally interrupts on seven priority levels are supported, when no onboard interrupts are used. If onboard interrupts are used, for example interrupts from the serial ports (ACIAs) or timers etc, then interrupts on some of the priorities are reserved. In this case the internal interrupts are used as auto-vectored interrupts. All the options for interrupt usage are set by jumpers.

The CPU card was thoroughly tested in lab and deployed for regular use in some of the Indus-1 control sub systems.

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A.6: X-Ray beam position monitor on Indus-2

X-ray beam position monitors (XBPM) are widely used for photon beam diagnostics in SR source facilities. They give sub-micron accuracy in beam position and micro-rad sensitivity in its angular divergence. A staggered pair XBPM based on photoelectron emission principle is designed, developed in Indus Synchrotron Utlisation Division and installed on Indus-2 frontend of bending magnet beamline BL-12. The vertical beam position is calculated by measuring asymmetry in currents between four detector blades. The principle and schematic of staggered XBPM is shown in Fig. A.6.1(a) and 1(b) respectively. Fig. A.6.1(c) shows the photograph of installed XBPM on BL-12 frontend, 10^0 port in DP-5 of Indus-2 at a distance of 4.95m from the tangent point. The formulae for determining vertical beam position are given in reference [V.P. Dhamgaye et al., Proceedings of DAE-BRNS InPAC 2009, RRCAT (2009)].

Calibration: XBPM is calibrated by two schemes: (1) by scanning the XBPM in the vertical direction in stationary path of the SR beam and (2) by giving controlled bump to electron beam keeping XBPM fixed. First scheme has given the calibration curve and second scheme has helped to check the linearity of the system.

Beam Stability: The beam position stability between injection to injection (storage to storage) have been observed for intraday and compared with other days. Fig. A.6.2 shows the intraday beam stability consisting of 8 injections and 2 storage events. All injections except 7 are within the 110μm position value. During the injection 7, there was a problem reported with one of the quadrupole power supply which resulted in beam position shift during the injection process. The two storage (s1-s2) beam positions are different because of the reported problem in quadrupole settings.

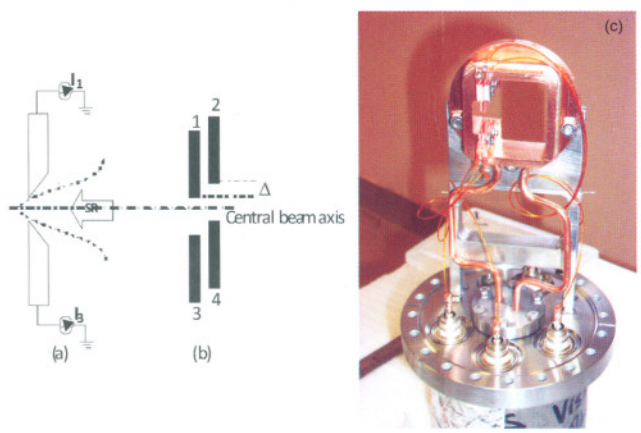

Fig. A.6.1: (a) XBPM principle (b) staggered pairs of blades fixed at known distances from centre of gravity of SR (c) photograph of installed XBPM on BL-12.