A.7: Low jitter FPGA based VME delay generator board

A four layer Versa Module Euro (VME) delay generator board has been designed and developed for future accelerators. This is a field programmable gate array (FPGA) based delay board. It gives multiple delayed trigger outputs (O/P) with low timing jitter (10s of ps).

Board features: Main features of the board are: Standard VME bus interface (A24:D16), Form factor: 6U & single slot, both external & on-board clock interface, pin programmable clock selection, delay resolution is 10 ps and jitter is ~ 10s of ps, one external trigger input (I/P) & 5 trigger O/P, I/P trigger is fed with optical isolation, each O/P gives delayed trigger pulse with respect to I/P trigger pulse, delay of each O/P is remotely adjustable in coarse and fine time scale, coarse scale - as per the clock frequency, fine scale - 10 ps, trigger O/Ps are in two forms- electrical form: low voltage transistor-transistor logic (LVTTL), fibre optic (FO) form: FO transmitter O/P is for plastic optical fibre (POF) interfacing, board supports RS-485 based interfacing also for standalone operation.

Description: The board is shown in Figure A.7.1. It is designed with high speed logic circuits for handling high frequency differential clock and O/P trigger pulse signals. External high frequency RF clock is handled via differential 50 ohm lines, high speed logic circuits for its scaling and direct interfacing to Spartan-3 FPGA clock I/Ps. 125 MHz on-board oscillator is also interfaced to FPGA. It has selectable clock feature. The O/P trigger pulse is generated at the specific delayed instant as per the set data. Delay data of each channel is stored in particular register. This can be set via VME as well as by RS-485 interface. Coarse delay of each O/P is generated by the synchronous counter within FPGA. Coarse delay resolution is governed by the external/on-board clock frequency, being used for counter. Delayed trigger pulses from FPGA are available at coarse delay time scale. These signals are handled via LVPECL logic circuits for interfacing with external precision delay line ICs, which gives delay in fine time scale of few nano seconds range with delay step in 10 ps. Differential O/P from fine delay IC is converted into 1:2 fanout single ended O/Ps. One of these is electrical O/P of LVTTL level. Other one is converted into fibre optic based output for plastic optical fibre interface. Isolated RS-485 serial interface is provided for its access in standalone mode to select particular channel and set delay data.

Testing: High frequency external RF signal is provided to the board from RF generator. 1 Hz I/P trigger is fed from function generator. Presently external RF signal of 505 MHz (like Indus-2 RF) is applied. Five trigger O/Ps are observed at both electrical and FO version. Existing FO receiver card is used for checking the performance. Coarse, fine delays of each trigger O/P, delay resolution of each channel & timing jitter are checked. Timing jitter between two channels at the electrical O/P is < 40 ps (Fig. A.7.2). The same is observed between two FO receivers O/Ps. It is < 80 ps. (Fig. A.7.3). Board has been tested successfully in laboratory with both VME and RS-485 interfaces. This board may be used for low timing jitter application in future accelerators.

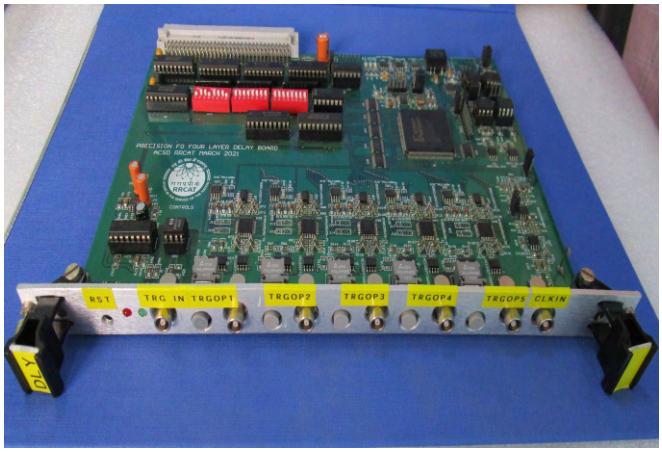

Fig. A.7.1: Low jitter VME delay generator board.

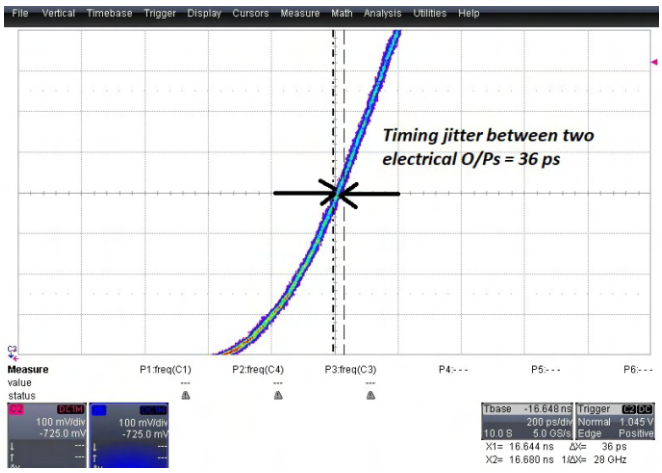

Fig. A.7.2: Timing jitter between electrical O/Ps.

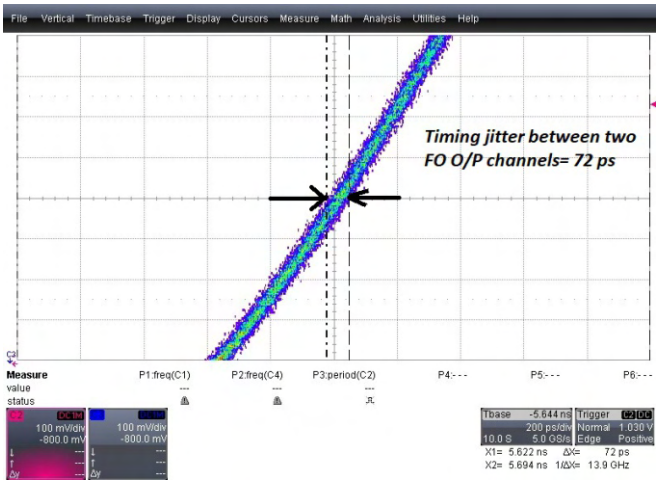

Fig. A.7.3: Timing jitter between FO receiver O/Ps.

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